# Module Announcement

## PhD in Information Technology and Electrical Engineering

## Università degli Studi di Napoli Federico II

## Module Title: Safety Critical Systems for Railway Traffic Management


## Lecturer: Mario Barbareschi

**Rete Ferroviaria Italiana, Gruppo delle Ferrovie dello Stato Italiane**
**Ricerca e Sviluppo – Sviluppo Sistemi**
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**CV:** Mario Barbareschi received the Ph. D. in Computer and Automation Engineering in 2015 and the Master Degree in Computer Engineering cum laude in 2012, both from the Università degli Studi di Napoli Federico II, Italy, where he worked a post-doctoral fellow until 2019. He is currently employed in Rete Ferroviaria Italiana, member of Gruppo Ferrovie dello Stato Italiane, where he is currently working as senior embedded technology specialist.

## Dates and Locations (rooms are in 3A Building, via Claudio 21, Napoli)

| Date | Hours | Room |
|---|---|---|
| 10nd January 2020 | **9:00-13:00** | **TBD** |
| 13th January 2020 | **13:00-16:00** | **TBD** |
| 17th January 2020 | **9.00-13.00** | **TBD** |
| 20nd January 2020 | **13:00-16:00** | **TBD** |
| 24th January 2020 | **9:00-12:00** | **TBD** |
| 27th January 2020 | **13:00-16:00** | **TBD** |

## Content

**I Lesson - Introduction** (fino a 250 car.):

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The Italian railway system from different points of view: structure of Ferrovie dello Stato and Rete Ferroviaria Italiana. Research and Deploy activities in railway signaling systems, projects and innovation activities.

**II Lesson – Computing Architectures** (fino a 250 car.):
Fail-safe computing architectures for railway applications: real-time system, 2oo2 architectures, consensus managing, vital and fail-safe output. Model-based approaches for critical software. Laboratory: Matlab Simulink.

**III lesson – Security Standards** (fino a 250 car.):
Principles of EN 50126, EN 50128 and EN 50129. Software artifacts and V model: SRS, testing plan, design and implementation of critical software. The fundamental role of coding standards for programming languages. MISRA C at a glance and hands-on. Laboratory: Matlab Polyspace.

**IV Lesson – Coding a Real-time Operating System - Part 1** (fino a 250 car.):
Completion of documentation, software implementation and testing of an RTOS for ARM Cortex M3 Architecture (ARMv7-M). Asynchronous and synchronous interprocess communication. Laboratory: git, continuous integration, cross compilation and debugging, SystemWorkbench for STM32 devices.

**V Lesson - Coding a Real-time Operating System - Part 2** (fino a 250 car.):
Device driver for external communication, application development: deadline, priority and period of critical tasks. Laboratory: git, continuous integration, cross compilation and debugging, SystemWorkbench for STM32 devices.

**VI Lesson – Model Based Design** (fino a 250 car.):
Model based engineering of critical systems. Simulation and testing. From model to software in Matlab Simulink.

## ECTS Credits: 3.3

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## Notes

Doctoral Students are requested (starting from Lesson II) to bring their own notebook with SystemWorkbench AC6, Git, Word Processor, Spreadsheet tool, licensed Matlab with Polyspace toolboxes installed. A STM32 development board will be distributed to all attendees.

Doctoral Students with noticeable experience on embedded system, C coding, RTOS and Matlab Simulink can participate as Tutors. In particular, Tutors can be involved as assistants during last 4 lessons.

Participant to the Module (including those interested to the Tutorship positions) are strongly encouraged to e-mail to the lecturer, specifying in the subject the name of this course name, while in the body their name, master degree and a really short description of their research activities.

Info: **Prof. Antonino MAZZEO -** tel. 081 7683904 – antonino.mazzeo@unina.it
**Prof. Nicola MAZZOCCA -** tel. 081 7683815 – nicola.mazzocca@unina.it